SECTION III—REMARKS

This amendment is submitted together with a Request for Continued Examination (RCE) in response to the final Office Action mailed June 29, 2005, the Advisory Action mailed September 23, 2005, and the Notice of Appeal mailed by Applicants on September 29, 2005.

No claims are amended herein, and claims 1, 3-12, 14-23, 25-28 and 30-32 remain pending in the application. Applicants respectfully request reconsideration of the application and allowance of all pending claims in view of the above amendments and the following remarks.

Rejections Under 35 U.S.C. § 103

The Examiner rejected claims 1, 3-12, 14-23, 25-29 and 30-32 under 35 U.S.C § 103(a) as obvious in view of, and therefore unpatentable over, different combinations of the following references: U.S. Patent No. 4,939,694 to Harrington *et al.* ("Harrington"); U.S. Patent No. 6,088,740 to Ghaffari *et al.* ("Ghaffari"); U.S. Patent No. 4,366,536 to Kohn ("Kohn"); and U.S. Patent No. 6,567,862 to Saito ("Saito").

Applicants respectfully traverse the Examiner's rejections. To establish a *prima facie* case of obviousness, three criteria must be met: (1) the prior art references must teach or suggest all the claim limitations; (2) some suggestion or motivation to combine the references must be found in the prior art; and (3) there must be a reasonable expectation of success. MPEP § 2143. Applicants

respectfully submit that, as explained below, the Examiner has not established a *prima facie* case of obviousness.

Claims 1, 12, 23 and 28 are not obviated by Harrington in view of Ghaffari

Claim 1 recites a method combination including issuing a plurality of commands to a controller, wherein the commands are issued in a first order and wherein "each command includes a command, a memory address identifying a memory location to which the completion status will be written, and a value to be written upon completion of the command," and "indicating the completion status of commands in a second order, wherein the second order is different from the first order."

In the final Office Action, the Examiner conceded that Harrington does not disclose a combination wherein "each command includes a command, a memory address identifying a memory location to which the completion status will be written, and a value to be written upon completion of the command." Nonetheless, the Examiner alleged that Ghaffari discloses this limitation and concluded that it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Harrington and Ghaffari to arrive at the presently claimed invention.

In response to the final Office Action, Applicants argued that Ghaffari does not, as the Examiner alleged, teach that each command includes a command, a memory address identifying a memory location to which the completion status will

be written, and a value to be written upon completion of the command. Instead, as indicated in the passages referenced by the Examiner (Fig. 5; col. 7, lines 24-25 and 45-50) Ghaffari teaches only providing an address where the results of a given data operation should be placed. By "results of a given data operation" Ghaffari clearly means the target data retrieved, stored, or otherwise acted upon by the command, not any kind of completion status indication associated with the command. Completion status is not a "result of a given data operation," as this phrase is used in Ghaffari. Completion status is rather an indication to the controller that the issued command has been completed. Ghaffari thus does not disclose, teach or suggest that its commands include "a memory location to which the completion status will be written, and a value to be written upon completion of the command."

In the Advisory Action, the Examiner responded to Applicants' arguments as follows:

> Applicant argued in substance that:
>
> (1) "Completion status in [*sic*] not a "result of a gine [*sic*] data operation", as this phrase is used in Ghaffari . . . Ghaffari does not disclose [sic], teach of suggest that is [*sic*] commands include a memory location to which the completion status will be written, an [*sic*] a value to be written upon completion of the command".
>
> Examiner respectfully disagreed with Applicant's remarks:
>
> As to the point (1), Ghaffari teaches the next register that contains the address of a completed command (col. 2, ln. 34-36). In additional [*sic*], Harrington teaches the format of PIO commands . . . the register 14A and 14B contain the PIO code and a return bit. . . A selectd [*sic*]

> bit (e.g., bint [*sic*] 0) or registrer [*sic*] 14A conbe [*sic*] used to indicate whether the address is a physical address (bit 0=0) or a logical address (bit 0=1). The return bit R determines whether the controller will generate a synchronous interrupt when the PIO have been completed, col 11, ln 30-40 and ln 43-42-48/load status interrupt return information into status registers 15. Interrupts in the system described [*sic*] can be . . . the latter occurring when the controller completes a PIO command (col 11 ln 51-58).

Even if everything the Examiner alleges regarding Ghaffari is true, it is immaterial. Why? Because what the Examiner alleges Ghaffari discloses is not what the claim recites. The Examiner alleges that Ghaffari teaches "the next register that contains the address of a completed command," but this is almost the exact opposite of what the claim recites. The claim recites a command that includes an address identifying a memory location to which the completion status will be written. In contrast, what the Examiner points out is the reverse of what is claimed—that a register contains the address of a completed command. These two statements are different because they involve different content in different memory locations. Ghaffari therefore cannot disclose, teach or suggest a combination wherein "each command includes a command, a memory address identifying a memory location to which the completion status will be written, and a value to be written upon completion of the command."

Despite the Examiner's concession that Harrington does not disclose a combination wherein "each command includes a command, a memory address identifying a memory location to which the completion status will be written, and a value to be written upon completion of the command," Applicant's legal

representative understands the Examiner to now be arguing that Harrington does disclose such a limitation. But as with Ghaffari, the passages the Examiner quotes from Harrington are immaterial because they are not what the claim recites.

Harrington's statement that "[a] selected bit (e.g., bit 0) of register 14A can be used to indicate whether the address is a physical address (bit 0=0) or a logical address (bit 0=1)" is immaterial because the addresses that bit 0 indicates are physical or logical are not memory addresses identifying a memory location to which the completion status of the command will be written. Contrary to the Examiner's assertion, figure 8 and associated text indicate that the addresses that appear with the PIO commands are not addresses identifying a memory location to which the completion status of the command will be written. Instead, they are addresses of something completely different, such as addresses of a control block in the main memory.

As to Harrington's statement that "[t]he return bit R determines whether the controller will generate a synchronous interrupt when the PIO command has been completed (R is set) or whether such interrupt is not generated (R is not set)," it is similarly immaterial because the return bit R determines only whether an interrupt is synchronous or asynchronous. This language from Harrington says nothing about whether the PIO command includes "a memory address identifying a memory location to which the completion status will be written, and a value to be written upon completion of the command."

Finally, as to Harrington's statement that "[t]he I/O controller loads interrupt return information into status registers 15" is also immaterial. Even if interrupt return information is written to status registers 15, as pointed out above nothing in Harrington indicates that the command registers for the PIO commands include the memory address of status registers 15—in other words, the PIO commands do not include "a memory address identifying a memory location to which the completion status will be written, and a value to be written upon completion of the command."

Since neither Harrington nor Ghaffari disclose the claimed limitation, Applicants submit that, when combined, Harrington and Ghaffari cannot disclose, teach or suggest every element of the claimed combination. Applicants respectfully request withdrawal of the rejection and allowance of the claim.

Claim 12 recites an article of manufacture comprising a machine-readable medium having instructions stored thereon to issue a plurality of commands from a controller, wherein the commands are issued in a first order and "wherein each command includes a command, a memory address identifying a memory location to which the completion status will be written, and a value to be written upon completion of the command," and "indicate the completion status of commands in a second order, wherein the second order is different from the first order." By analogy to the discussion above for claim 1, Harrington and Ghaffari, alone or in combination, do not disclose, teach or suggest a combination including the recited limitations. Applicants submit that claim 12 is therefore allowable and respectfully request withdrawal of the rejection and allowance of the claim.

Claim 23 recites an apparatus including a controller adapted to accept a plurality of commands, wherein the commands are issued in a first order and "wherein each command includes a command, a memory address identifying a memory location to which the completion status will be written, and a value to be written upon completion of the command," and "wherein a completion status of each command is indicated in a second order, and wherein the second order is different from the first order." By analogy to the discussion above for claim 1, Harrington and Ghaffari, alone or in combination, do not disclose, teach or suggest a combination including the recited limitations. Applicants submit that claim 23 is therefore allowable and respectfully request withdrawal of the rejection and allowance of the claim.

Claim 28 recites a system including a controller adapted to accept a plurality of commands issued in a first order and "wherein each command includes a command, a memory address identifying a memory location to which the completion status will be written, and a value to be written upon completion of the command," a plurality of computational units to execute the plurality of commands, and a memory, "wherein a completion status of commands is written to the memory in a second order, and wherein the second order is different from the first order." By analogy to the discussion above for claim 1, Harrington and Ghaffari, alone or in combination, do not disclose, teach or suggest a combination including the recited limitations. Applicants submit that claim 28 is therefore allowable and respectfully request withdrawal of the rejection and allowance of the claim.

Claims 3-11, 14-22, 25-27 and 30-32 are not obviated by Harrington combined with Ghaffari, Kohn or Saito

If an independent claim is non-obvious under 35 U.S.C. § 103, then any claim depending therefrom is also non-obvious. MPEP § 2143.03; *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). As discussed above, independent claims 1, 12, 23 and 28 are in condition for allowance. Applicants therefore respectfully submit that claims 3-11, 14-22, 25-27 and 30-32 are allowable by virtue of their dependence on allowable independent claims, as well as by virtue of the features recited therein. Applicants therefore respectfully request withdrawal of the rejections and allowance of these claims.

Conclusion

Given the above amendments and accompanying remarks, all claims pending in the application are in condition for allowance. If the undersigned attorney has overlooked a teaching in any of the cited references that is relevant to allowance of the claims, the Examiner is requested to specifically point out where such teaching may be found. Further, if there are any informalities or questions that can be addressed via telephone, the Examiner is encouraged to contact the undersigned attorney at (206) 292-8600.

Charge Deposit Account

Please charge our Deposit Account No. 02-2666 for any additional fee(s) that may be due in this matter, and please credit the same deposit account for any overpayment.

Respectfully submitted,

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Date: 11-28-05

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